WBS 6.6.3.3: CSM Technical Overview

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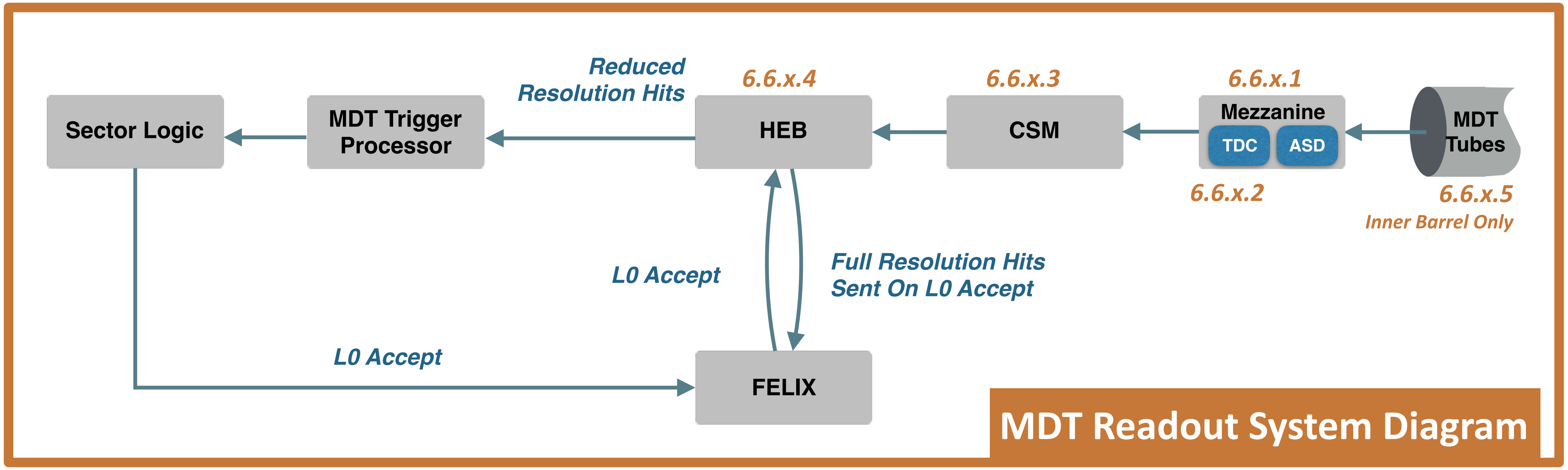
Conceptual Design Review for the High Luminosity LHC Detector Upgrade
National Science Foundation
Arlington, Virginia
March 8-10, 2016

Expertise

- Tom Schwarz, WBS 6.6.3.3
  - Assistant Professor at the University of Michigan
  - Current Level 2 Construction Manager for the HL-LHC Upgrade of the Muon Spectrometer
  - Project Lead for the sTGC trigger signal packet router for the Phase I upgrade of the ATLAS new small wheel
  - BSE and MSE in Electrical Engineering
  - 3 years of experience with silicon micro-machining, RF engineering, and microwave circuitry design

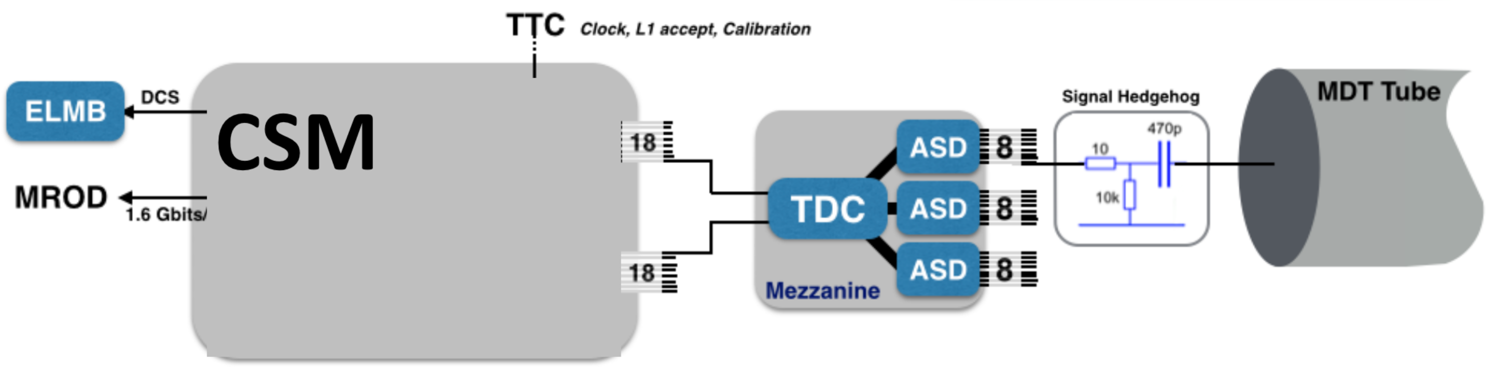
- University of Michigan
  - Long history of electronics development and commissioning
    - Developed three ASICs for previous collider experiments
    - Developed two FPGA-based boards including the previous CSM currently used for MDT readout and developing a similar board for the Phase I ATLAS upgrade (New Small Wheel).
    - Important role in MDT front-end commissioning.
    - Currently responsible for daily operation of the entire ATLAS MDT system (gas, calibration, electronics).

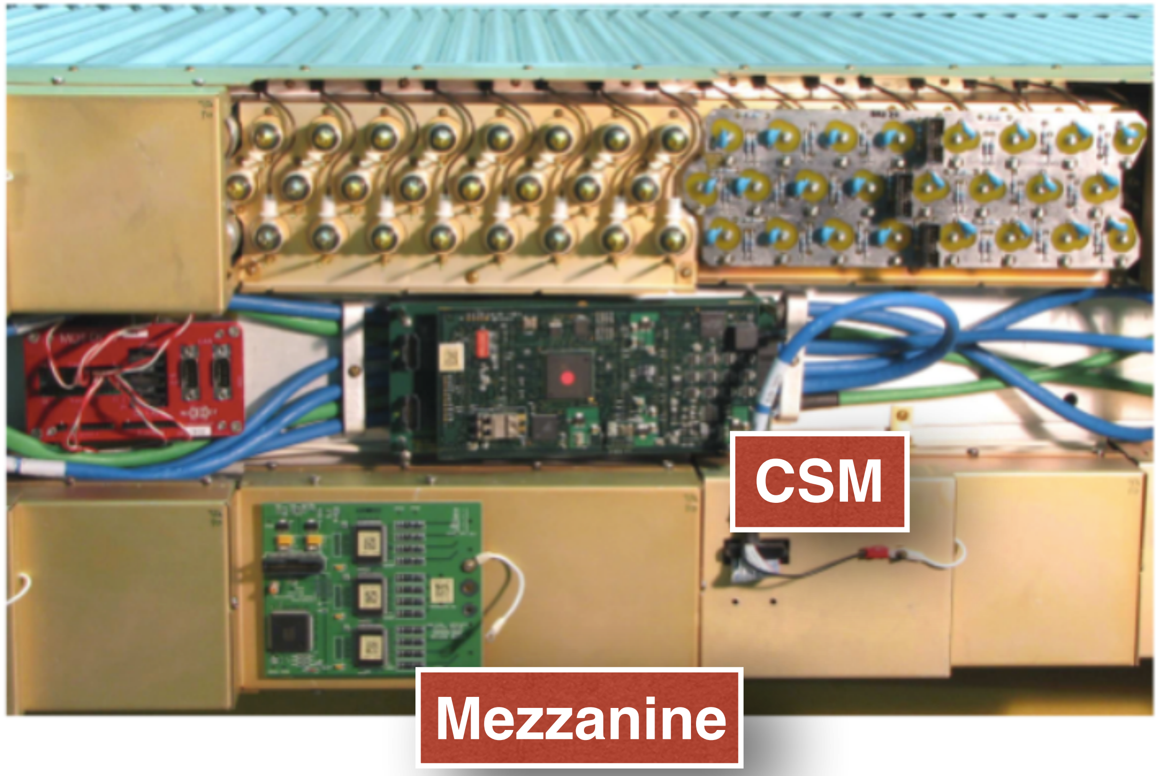
Summary of the NSF Scope

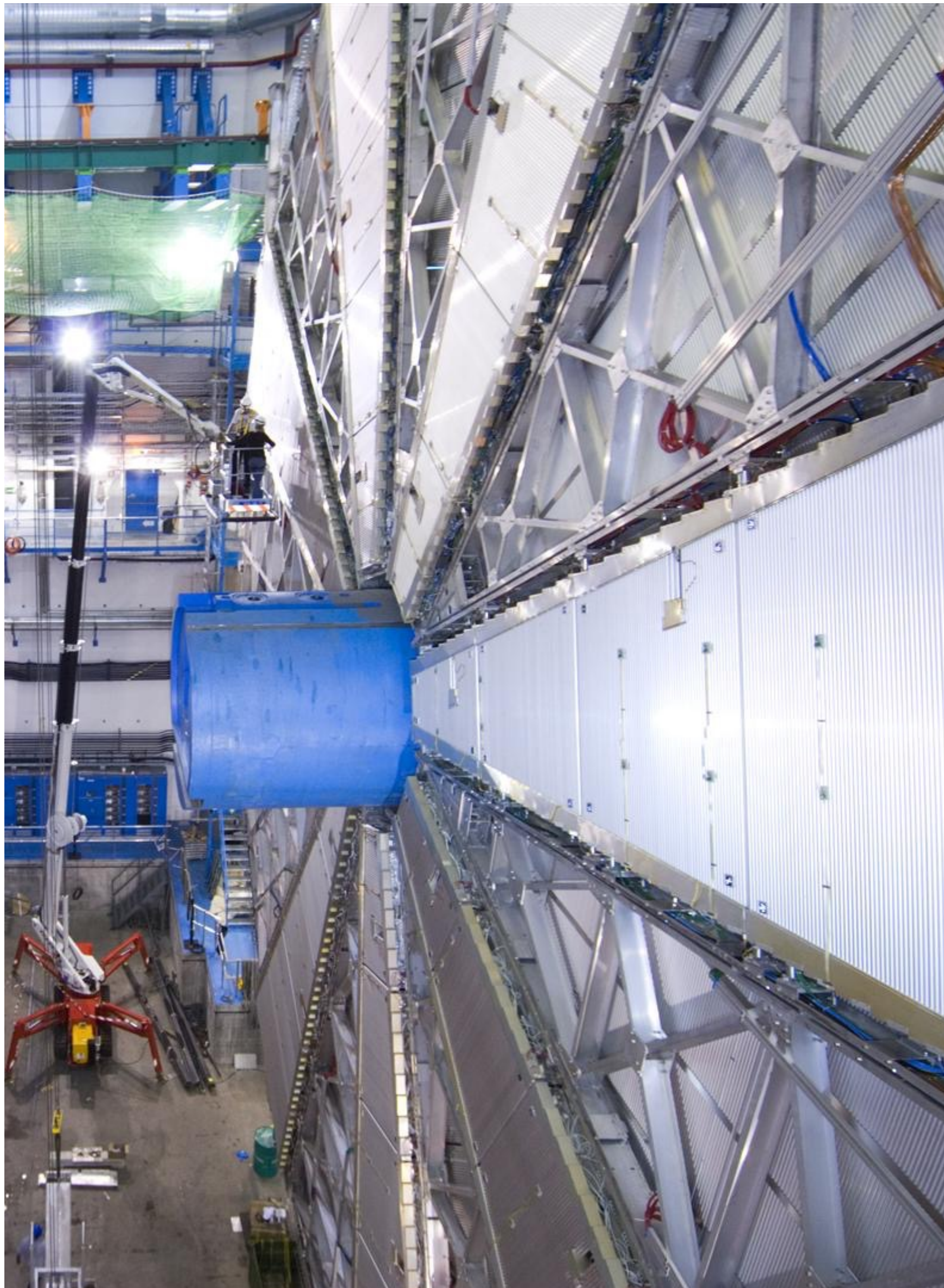


WBS	Deliverable	Functionality	# Produced by US	US Institutes	International Interests
6.6.x.1	**PCB for Mezzanine**	PCB board for the Mezzanine Card, which consists of three ASD and one TDC chips.	17,225 boards	University of Arizona ***6.6.1.1***	*none*
6.6.x.2	**Time-to-Digital Converter (TDC)**	Stores arrival times of the leading and trailing edges of the MDT signal (asic chip)	22,000 chips	University of Michigan ***6.6.3.2***	MPI (Collaborative), Japan
6.6.x.3	**Chamber Service Module (CSM)**	Data are formatted, stored, and sent via optical link to the Hit Extraction Board (HEB)	1300 boards	University of Michigan ***6.6.3.3***	*none*
6.6.x.4	**Hit Extraction Board (HEB)**	Sends reduced resolution hits to the trigger processor and on a Level 0 accept sends full resolution hits to FELIX for readout	24 boards	University of Illinois Urbana-Champaign ***6.6.4.4***	*none*
6.6.x.5	**sMDT**	Short monitored drift tubes to be paired with new RPC's on inner barrel for trigger	48 chambers	Michigan State University (tubes) ***6.6.5.5*** University of Michigan (chambers) ***6.6.3.5***	MPI and Protovino (Collaborative - 50%)

Current MDT Front-End

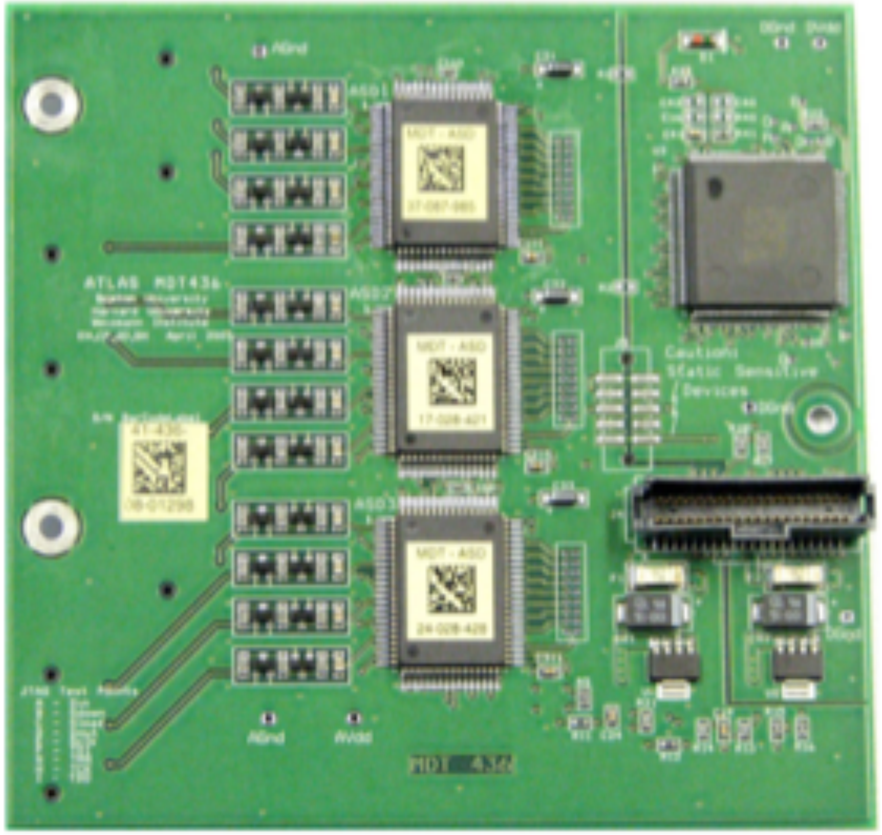


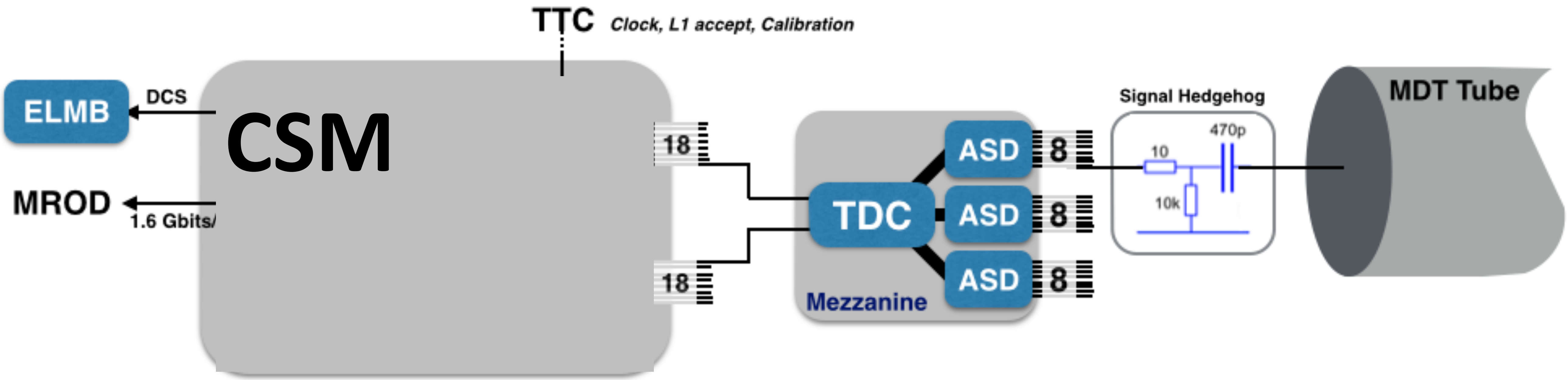




Current MDT Front-End

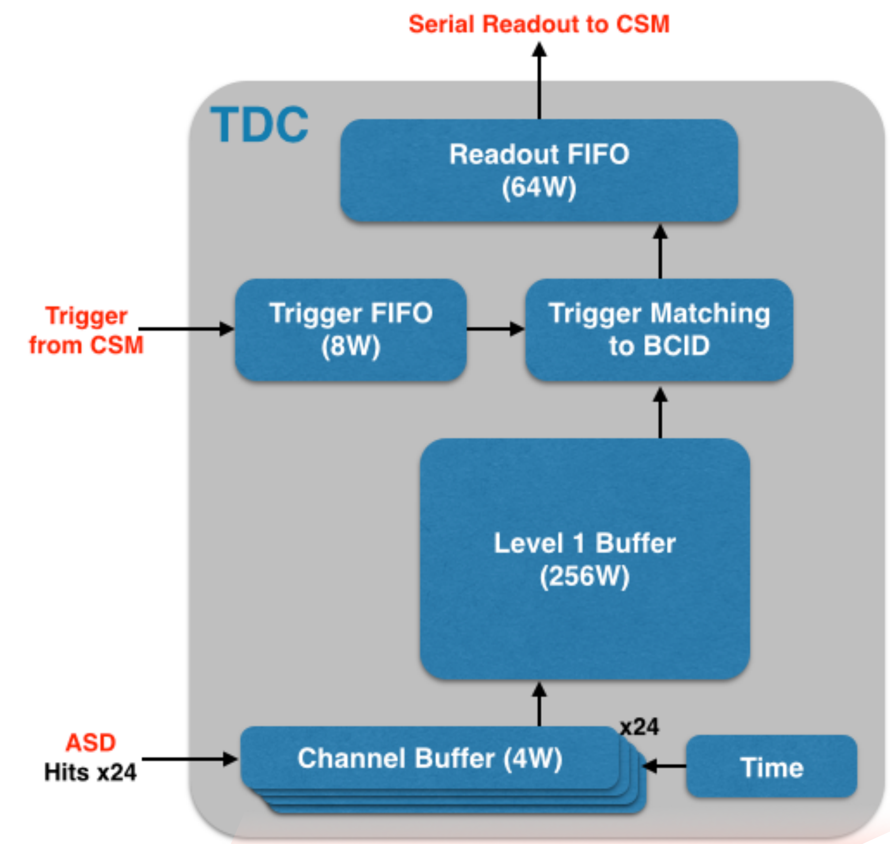
- The raw drift signals for up to 24 tubes are amplified, shaped and digitized by three ASD chips, and routed to a Time-to-Digital Converter (TDC) on mezzanine
- TDC stores the arrival times of the leading and trailing edges of the signal, as well as an identifier word for the corresponding tube
- Times are measured in units of the Timing, Trigger and Control (TTC) clock, which operates at the bunch crossing frequency of the LHC (40.08 MHz)

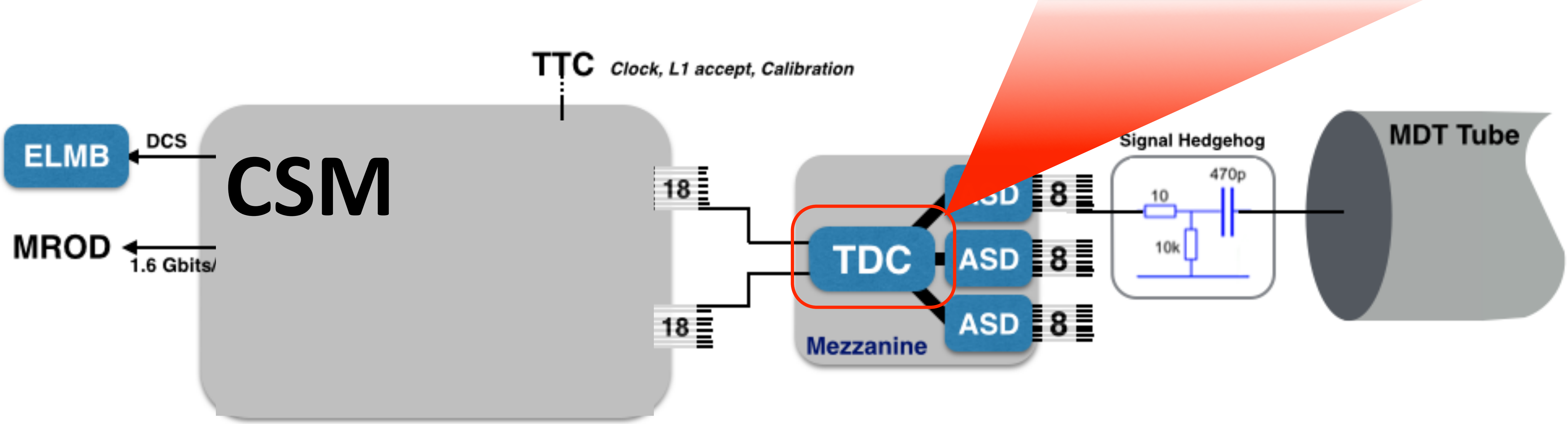




Current MDT Front-End

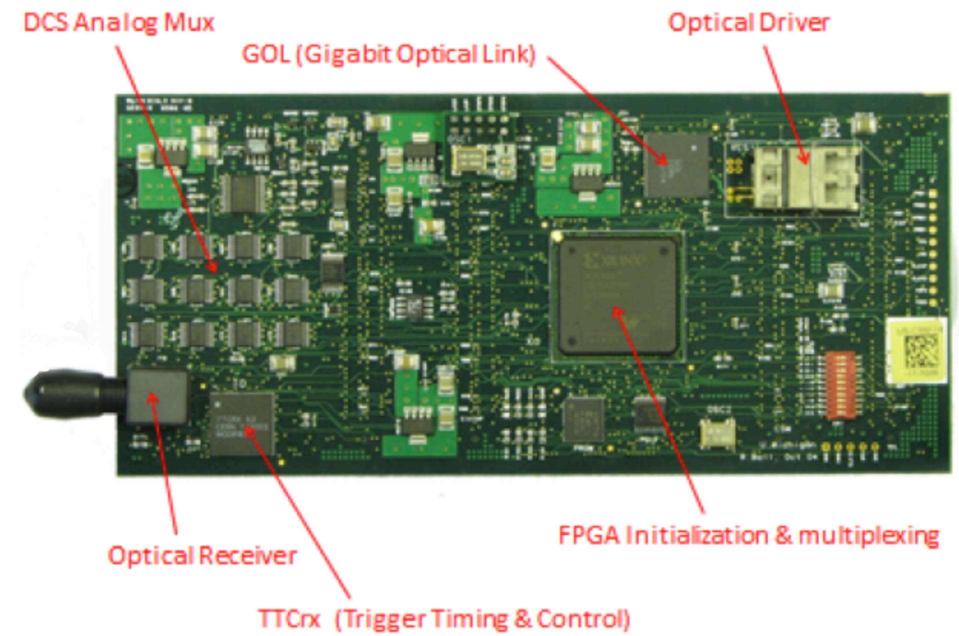
- Current TDC stores arrival times of leading & trailing edges of tube signals, as well as an identifier word for the corresponding tube, in a buffer memory of 256 words
- Timing for triggered hits are matched to corresponding bunches and passed to a readout FIFO to be sent to the CSM

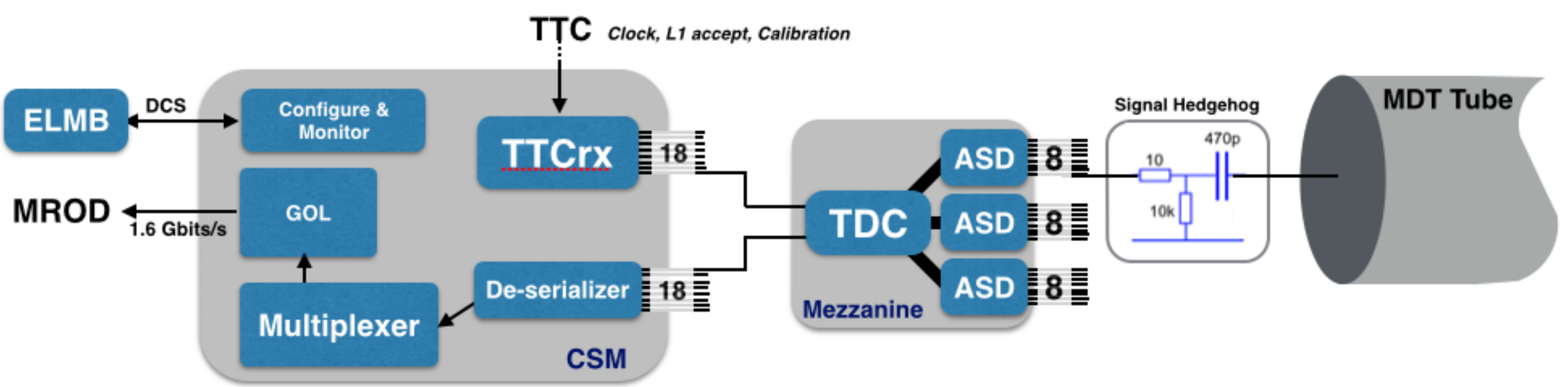




Current CSM

- One MDT chamber, up to 18 mezzanines, are controlled by a local processor board (CSM)
- The CSM broadcasts the TTC signals to the TDCs, and collects data from the TDCs on Level-1 accept
- At the CSM, data are formatted, stored, and sent via optical link to the MDT readout driver modules (MROD).
- MROD assembles the data for each event and transfers it to Readout Buffer (ROB), where data are stored until accepted/rejected by Level-2 trigger.



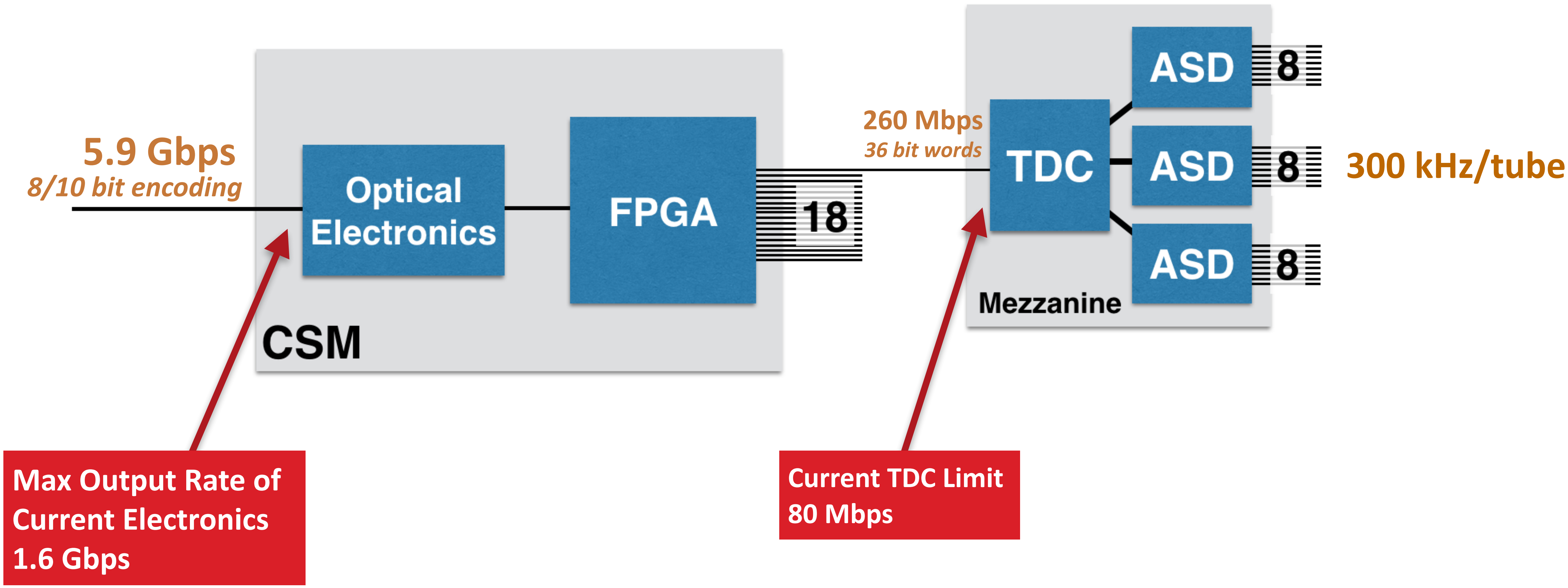


The Problem

To cope with high rates and 1 MHz trigger

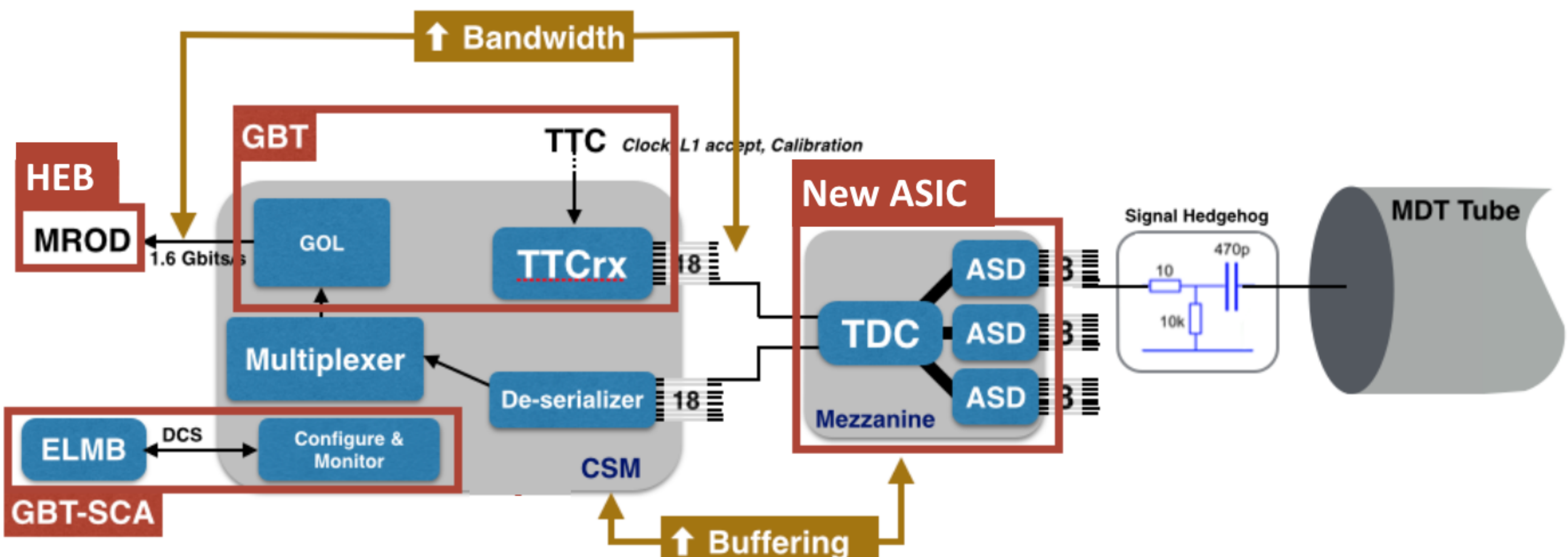
➡ The readout electronics of the MDT system must be replaced

Raise maximum MDT electronics rate to 300 kHz/tube



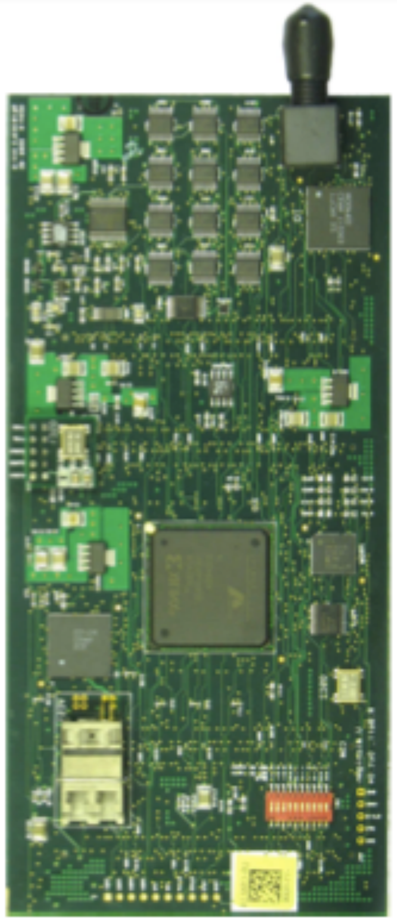
HL-LHC System Changes

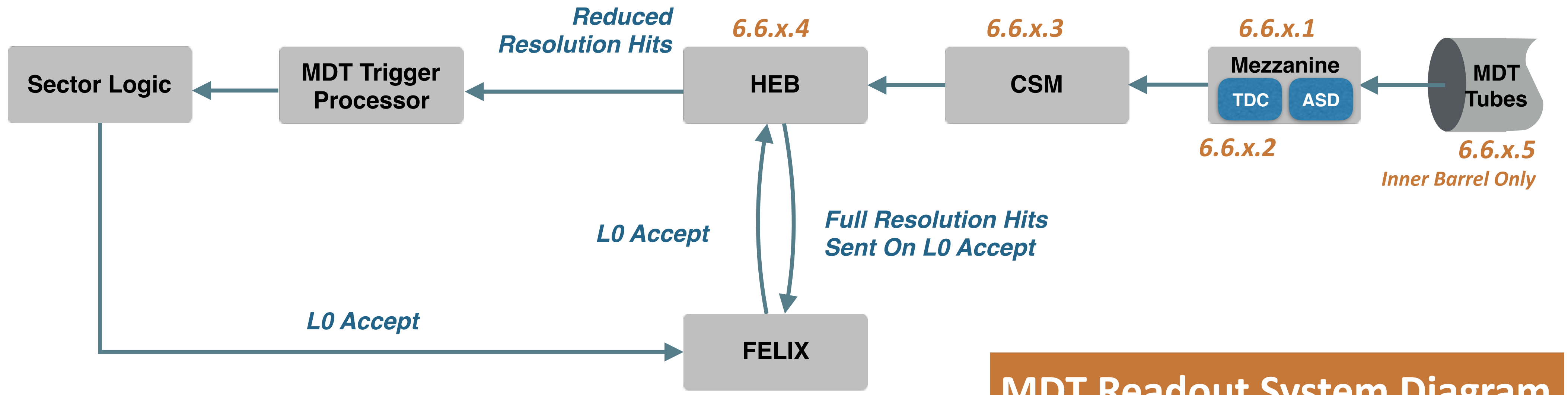
- ➡ Higher bandwidth from TDC's to CSM and CSM to USA15 and deeper buffers for mezzanine and CSM to handle the higher rates and longer latencies
- ➡ Need to handle new trigger path - MDT data must get out to USA15 before Level-0 decision
- ➡ Timing, Trigger, and Control (TTC) and GOL will be replaced by CERN GBT system
- ➡ Configure and Monitoring performed by GBT-SCA
- ➡ Front-end link exchange system (FELIX) will replace ROD-ROS to perform data collection from CSM. HEB will be used for hit reduction.



6.6.x.3 The HL-LHC CSM

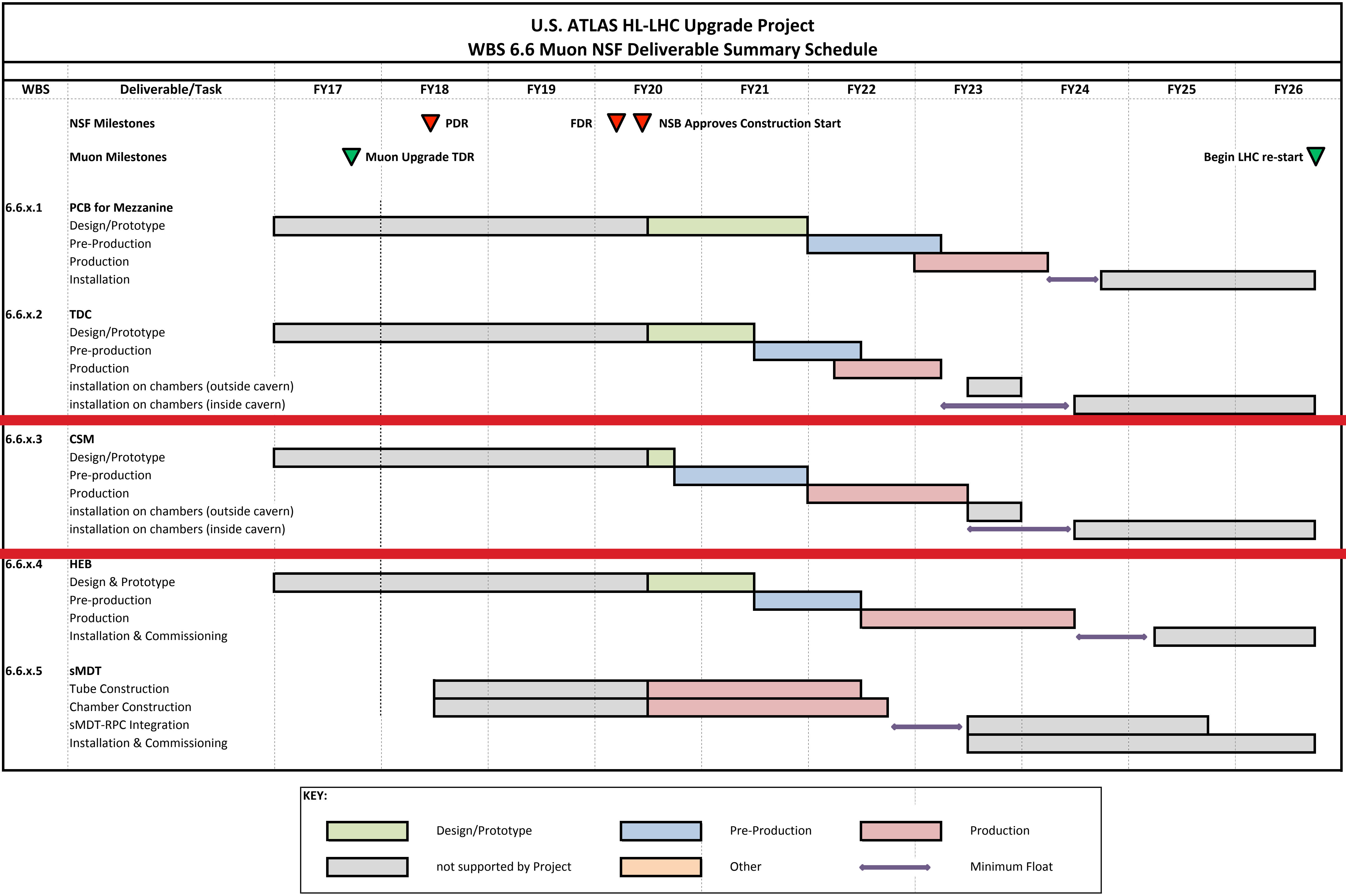
- Up to 18 mezzanine cards will still be controlled by the Chamber Service Module (CSM)
- The CSM broadcasts the control signals to the TDCs, and collects data from them
- At the CSM, data are formatted, stored, and sent via optical link to the Hit Extraction Board (HEB).
- 1300 CSM boards will be constructed by the University of Michigan (6.6.3.3). This represents 100% of the required CSM boards for ATLAS. There is no international competition.





MDT Readout System Diagram

Schedule


U.S. ATLAS HL-LHC Upgrade Project
WBS 6.6 Muon NSF Deliverable Summary Schedule
WBS
Deliverable/Task
FY17
FY18
FY19
FY20
FY21
FY22
FY23
FY24
FY25
FY26
NSF Milestones
PDR
FDR
NSB Approves Construction Start
Muon Milestones
Muon Upgrade TDR
Begin LHC re-start
6.6.x.1
PCB for Mezzanine
Design/Prototype
Pre-Production
Production
Installation
6.6.x.2
TDC
Design/Prototype
Pre-production
Production
installation on chambers (outside cavern)
installation on chambers (inside cavern)
6.6.x.3
CSM
Design/Prototype
Pre-production
Production
installation on chambers (outside cavern)
installation on chambers (inside cavern)
6.6.x.4
HEB
Design & Prototype
Pre-production
Production
Installation & Commissioning
6.6.x.5
sMDT
Tube Construction
Chamber Construction
sMDT-RPC Integration
Installation & Commissioning
KEY:
Design/Prototype
Pre-Production
Production
not supported by Project
Other
Minimum Float

R&D Overview

- The CSM needs to develop more advanced prototypes during R&D, as the construction timeline is slightly earlier due to the need to install electronics on-chamber for the sMDT's

- CSM R&D Plan:

  - <u>FY16-FY17</u> System Design and Simulation: Defining specifications and developing a system simulation to test various designs.

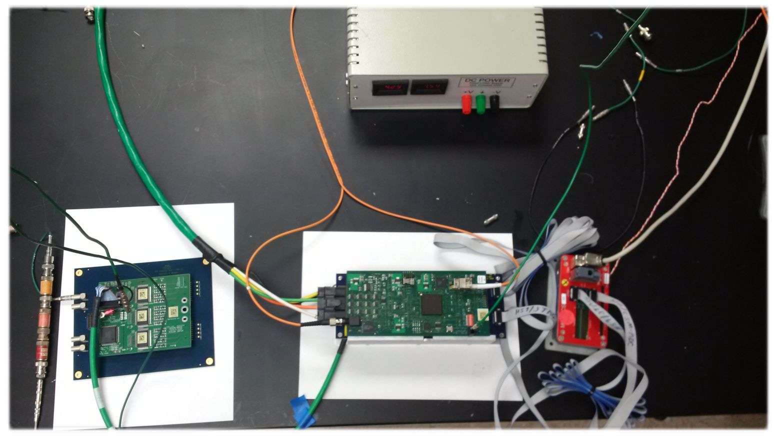
  - <u>FY16-FY17</u> Demonstrator: Developing a hardware-based implementation of the VHDL simulation in evaluation boards to test latency and rate capabilities.

  - <u>FY17-FY18</u> Prototype v1: First real board prototype utilizing a candidate FPGA, power chips, and the GBT-SCA chipset. Any candidate functionality will also be contained on the board.

  - <u>FY19-FY20</u> Prototype v2: Final production board before pre-production. Full testing with old mezzanine cards and new TDC chips.

R&D: Simulation

- Detailed electronics implemented in Behavioral Verilog or VHDL
- Validate simulation with test setup of current MDT system

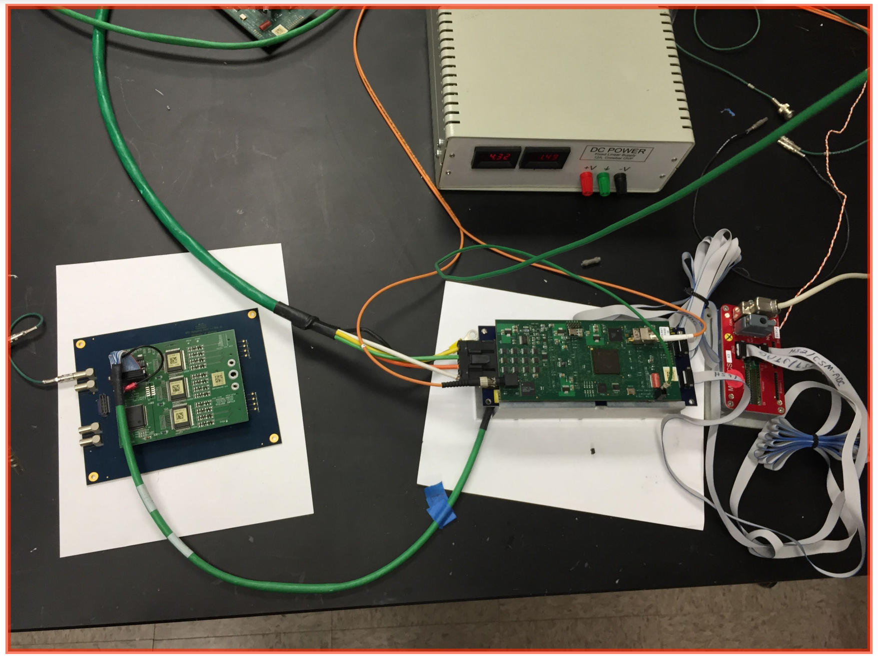


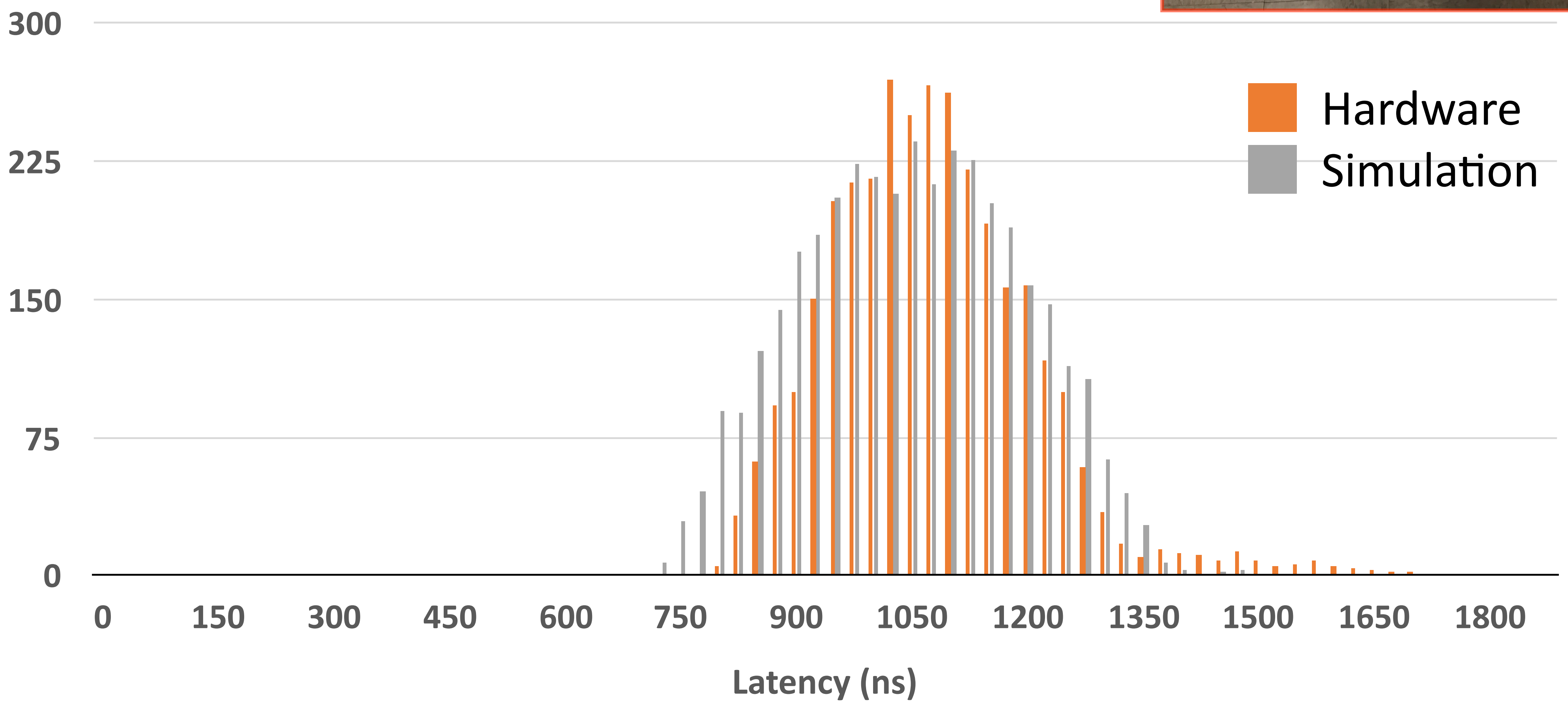
- Evaluate design performance for the predicted HL-LHC tube rates
  - ➡ Examine buffer occupancy at each stage in the data chain
  - ➡ Calculate travel time (latency) from original hit to USA15
  - ➡ Look at distribution of latency times for all rates anticipated

This was done for current MDT system, which behaves as designed

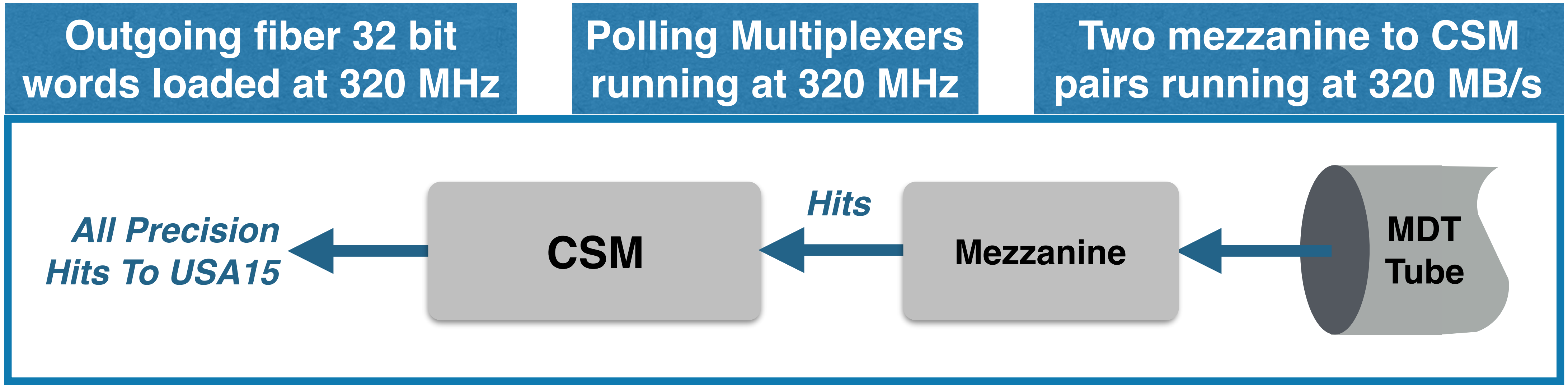
R&D: Hardware Tests

- Latency measured in test stand with 13 Mezzanine cards plugged into a single CSM
- Using very low hit rates
- Verifies simulation





R&D: Simulating HL-LHC System



- In this scheme, any MDT hits are sent off detector at full precision
- Several advantages to this system
    - Simple ➜ single path for trigger and data
    - All hits are selected, with no "trigger" window to create complications

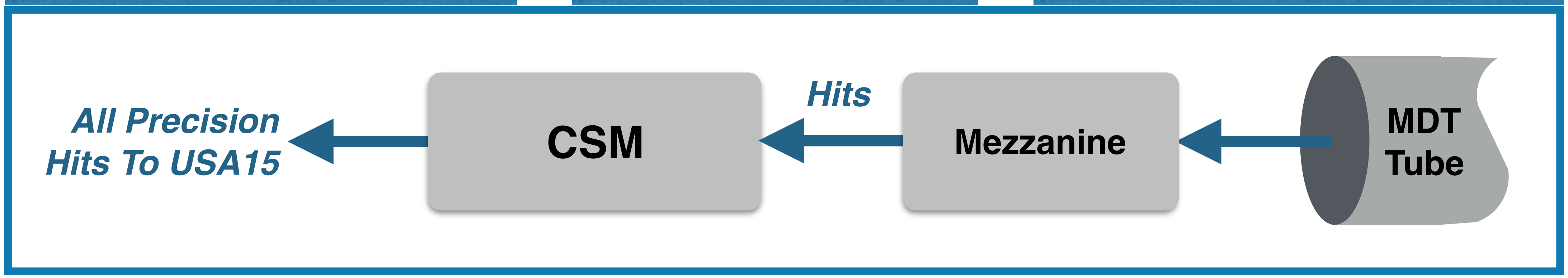
Key issue ➜ Can MDT hits be sent off fast enough to be included in the Trigger (< 6 μs) ?

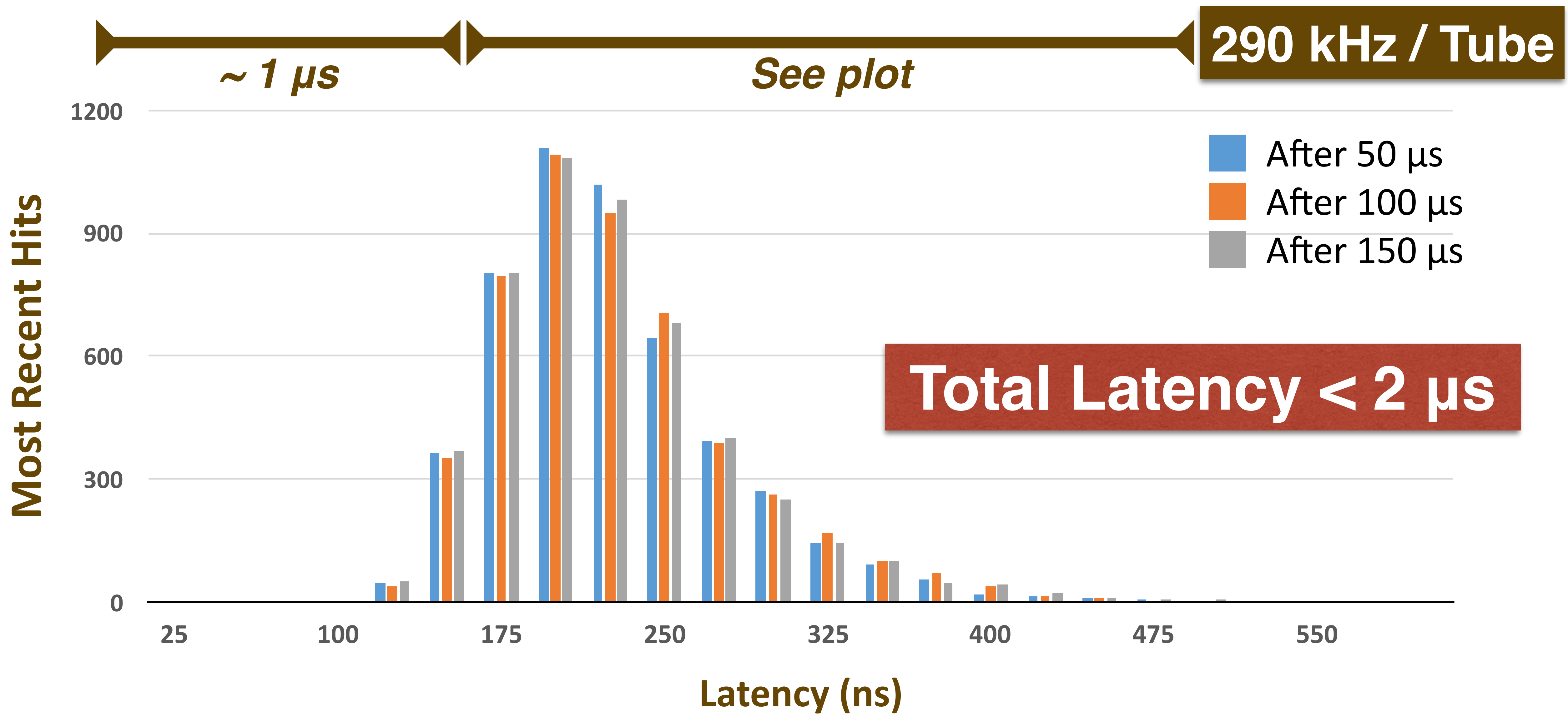
R&D: Simulating HL-LHC System

Outgoing fiber 32 bit words loaded at 320 MHz

Polling Multiplexers running at 320 MHz

Two mezzanine to CSM pairs running at 320 Mbps





CSM Costing: Labor (Michigan)

- <u>Basis of Estimate:</u> Expected personnel levels based on previous experience developing CSM at U-M

<u>Previous CSM Development Team at U-M</u>

- ➡ Jay Chapman (Sr Engineer equivalent) - CSM Leader/Firmware Design
- ➡ Pietro Binchi (Engineer) - Board design, left midway through development
- ➡ Bob Ball (Engineer) - CSM Firware, Board design, hired after Pietro left
- ➡ Tiesheng Dai (Engineer) - Test fixtures for MiniDAQ, test and debug
- ➡ Jon Ameel (Engineer) - Production, parts, testing on-site CERN
- ➡ Jeff Gregor and Tuan Anh Bui (Students) - Test and debug, some development

6.6 SUBSYTEM MUON: LABOR									
						Construction			
WBS	Tag	Description	FTEs	FY20 Q3,4	FY21	FY22	FY23	FY24	FY25
6.6.3.3		CSM		-	-	-	-		
		Design/Prototype		-	-	-	-		
			Sr Electronics Engineer	0.20					
			Jr Electronics Engineer	0.20					
			Electronics Technician	0.20					
			Engineering Student	0.20					
		Pre-production							
			Sr Electronics Engineer	0.30	1.00				
			Jr Electronics Engineer	0.30	1.00				
			Electronics Technician	0.30	1.00				
			Engineering Student	0.30	1.00				
		Production and Testing							
			Sr Electronics Engineer			0.45			
			Jr Electronics Engineer			0.45			
			Electronics Technician			1.00	0.50		
			Engineering Student			2.00	1.50		

CSM Costing: Labor (Michigan)

- <u>Basis of Estimate:</u> Expected personnel levels based on previous experience developing CSM at U-M

Sr Electronics Engineer	Lead on the CSM firmware and PCB design for two prototypes and production - for both new and legacy mezzanine electronics
Jr Electronics Engineer	Focus on modifications of new CSM to handle legacy mezzanine, test fixtures, and readout system
Engineering Technician	Lead development of movable test stations to test MDT chambers on surface, testing all new CSM's (> 1000)
Engineering Student	Assist with testing new CSM's, testing prototypes

6.6 SUBSYTEM MUON: LABOR										
						Construction				
	WBS	Tag	Description	FTEs	FY20 Q3,4	FY21	FY22	FY23	FY24	FY25
	6.6.3.3		**CSM**		-	-	-	-		
			Design/Prototype		-	-	-	-		
				Sr Electronics Engineer	0.20					
				Jr Electronics Engineer	0.20					
				Electronics Technician	0.20					
				Engineering Student	0.20					
			Pre-production							
				Sr Electronics Engineer	0.30	1.00				
				Jr Electronics Engineer	0.30	1.00				
				Electronics Technician	0.30	1.00				
				Engineering Student	0.30	1.00				
			Production and Testing							
				Sr Electronics Engineer			0.45			
				Jr Electronics Engineer			0.45			
				Electronics Technician			1.00	0.50		
				Engineering Student			2.00	1.50		

CSM Costing: Labor (Michigan)

- **Basis of Estimate:** Expected personnel levels based on previous experience developing CSM at U-M

L3	Inst/Position	Base Cost - 2016 (k$/year – burdened)	FY20 Q3,4	FY21	Hourly Rates FY22	FY23	FY24	FY25
3	**Michigan**							
	Proj Scientist	156,501.11	102.16	105.22	108.38	111.63	114.98	118.43
	Staff Scientist	95,155.20	62.11	63.98	65.89	67.87	69.91	72.00
	Sr Electronics Engineer	112,896	71.55	73.69	75.90	78.18	80.53	82.94
	Jr Electronics Engineer	93,542	59.28	61.06	62.89	64.78	66.72	68.72
	Electronics Technician	96,768	61.33	63.16	65.06	67.01	69.02	71.09
	Engineering Student	48,384	30.66	31.58	32.53	33.51	34.51	35.55
	Mechanical Engineer	119,992	76.04	78.32	80.67	83.09	85.59	88.15
	Mechanical Technician	96,768	61.33	63.16	65.06	67.01	69.02	71.09

Item	Description	AY k$	FY20	FY21	FY22	FY23	FY24	FY25	Total (k$)
6.6.3.3	**CSM - Michigan**	**Total**	**223.86**	**1687.87**	**364.02**	**155.77**			**2431.51**
		Labor	197.86	407.59	342.02	148.77			1096.23
		Material	20.00	1267.28	10.00	0.00			1297.28
		Travel	6.00	13.00	12.00	7.00			38.00
		CORE		1247.28					1247.28
		FTEs	2.00	4.00	3.90	2.00			11.90
	Design/Prototype	Total							0.00
		Labor	79.14	0.00					79.14
		Material	20.00						20.00
		Travel	6.00	6.00					12.00
		FTEs	0.80	0.00					0.80
	Pre-production	Total							0.00
		Labor	118.72	407.59	0.00				526.31
		Material		20.00					20.00
		Travel		7.00	2.50				
		FTEs	1.20	4.00	0.00				5.20
	Production & Testing	Total							0.00
		Labor		0.00	342.02	148.77			490.78
		Material		1247.28	10.00				1257.28
		Travel			9.50	7.00			16.50
		FTEs		0.00	3.90	2.00			5.90

CSM Costing: Construction

- **Starting point is the baseline HL-LHC design, including new FPGA and replacing some previous electronics with the GBT system of chips**
- **Assuming similar construction costs to the current ATLAS CSMs, accounting for new components, inflation, and exchange rates.**
- **Current CSM Construction costs taken from the 2003 ATLAS AGREEMENT 201-05 *"Production of CSM electronics for the ATLAS Muons Detector"***
- **New Components, such as the GBT chips, are taken either from recent listed costs or from estimates of the developer/manufacturer (CERN for GBT)**

Components	Count/Board	Cost/Item ($)	Basis of Estimate
CSM			
FPGA	1	279.323	Cost of modern FPGA matched to required performance
PROM	1	15.802	Scaled costs from 2003, plus inflation and exchange rate
GBLD, laser diode, housing	1	105.154	Current Cost estimates by CERN
GBT-SCA	1	33.649	Current Cost estimates by CERN
Misc Parts	1	175.015	Scaled costs from 2003, plus inflation and exchange rate
GBTx	1	175.000	Current Cost estimates by CERN
Fabrication and Assembly	1	157.400	Scaled costs from 2003, plus inflation and exchange rate
Cost per Board		**941.343**	
Basis of Number of Boards	**# Boards**	**Total Cost (k$)**	
624 chambers + 546 in end cap leads to 608, 510 CSM respectively. -64 CSM from NSW and +22 for new chambers. 10% overridge, 85% yield	**1325**	**1,247,279**	

Risks

Low risk. More detail in the BoE's, which we can go through during breakout. Below represent the largest risk for the CSM project.

Schedule Risk:

- **Probability:** Low
- **Potential Problem:** Some mezzanine cards in the detector will be unreachable and therefore cannot be replaced.
- **Mitigation:** Jr EE hired to handle CSM firmware modifications such that these chambers can still be read out with the new front-end system.

Please see Risk Registry in BoE for more